

CLAIMS

What is claimed is:

1. A high current, 5V tolerant buffer for operation at 2.5V or
5 less, comprising:

an inverter connected between a power supply voltage and ground;

a series connection of transistors between a PAD input and ground, an output of said inverter being input to a gate of one of said series connection of transistors, a gate of another of said series connection of transistors being connected to said power supply voltage, with a node N1 being formed between said series connection of transistors; and

a p-channel transistor between said power supply and said
15 node N1.

2. The high current, 5V tolerant buffer for operation at 2.5V or less according to claim 1, further comprising:

a comparator outputting a comparison between said power supply voltage and said PAD input voltage, an output of said comparator driving a gate of said p-channel transistor.

3. The high current, 5V tolerant buffer for operation at 2.5V or less according to claim 1, wherein:

said inverter comprises a series connection of a p-channel FET transistor and an n-channel FET transistor.

4. The high current, 5V tolerant buffer for operation at 2.5V or less according to claim 1, further comprising:

an input stage connected to said N1;
wherein said buffer is a bi-directional buffer.

5. The high current, 5V tolerant buffer for operation at 2.5V or less according to claim 1, wherein:

said buffer operates with a nominal power supply of 2.0V.

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6. The high current, 5V tolerant buffer for operation at 2.5V or less according to claim 1, wherein:

said buffer operates with a nominal power supply of 1.8V.

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7. The high current, 5V tolerant buffer for operation at 2.5V or less according to claim 1, further comprising:

a SCSI bus interface circuit connected to said buffer.

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8. The high current, 5V tolerant buffer for operation at 2.5V or less according to claim 1, further comprising:

a PCI bus interface circuit connected to said buffer.

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9. The high current, 5V tolerant buffer for operation at 2.5V or less according to claim 1, further comprising:

a PCMCIA bus interface circuit connected to said buffer.

10. The high current, 5V tolerant buffer for operation at 2.5V or less according to claim 1, wherein:

said buffer can sink at least 48 mA of current.

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11. A method of providing 5V tolerance to an output buffer operating at low voltage, comprising:

providing an inverter connected between a power supply voltage and ground;

5 providing a series connection of transistors between a PAD input and ground, an output of said inverter being input to a gate of one of said series connection of transistors, a gate of another of said series connection of transistors being connected to said power supply voltage, with a node N1 being formed between said series connection of
10 transistors;

providing a p-channel transistor between said power supply and said node N1; and

providing a power supply of no more than 2.5V nominal to said output buffer.

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12. The method of providing 5V tolerance to an output buffer operating at low voltage according to claim 11, further comprising:

providing an input stage connected to said buffer, said input stage having an input connected to said node N1;

20 wherein said buffer is a bi-directional buffer.

13. The method of providing 5V tolerance to an output buffer operating at low voltage according to claim 11, further comprising:

inputting a comparison between said power supply voltage and said PAD input voltage as an input to a gate of said p-channel transistor.

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14. The method of providing 5V tolerance to an output buffer operating at low voltage according to claim 11, wherein said step of providing a power supply comprises:

providing a nominal power supply of 2.0V.

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15. The method of providing 5V tolerance to an output buffer operating at low voltage according to claim 11, wherein said step of providing a power supply comprises:

providing a nominal power supply of 1.8V.

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16. The method of providing 5V tolerance to an output buffer operating at low voltage according to claim 11, wherein:

said buffer can sink at least 48 mA of current.

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17. Apparatus for providing 5V tolerance to an output buffer operating at low voltage, comprising:

means for providing an inverter connected between a power supply voltage and ground;

means for providing a series connection of transistors between a PAD input and ground, an output of said inverter being input to a gate of one of said series connection of transistors, a gate of another of said series connection of transistors being connected to said power supply voltage, with a node N1 being formed between said series connection of transistors;

means for providing a p-channel transistor between said power supply and said node N1; and

means for providing a power supply of no more than 2.5V nominal to said output buffer.

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18. The apparatus for providing 5V tolerance to an output buffer operating at low voltage according to claim 17, further comprising:

means for inputting a comparison between said power supply voltage and said PAD input voltage as an input to a gate of said p-channel transistor.

19. The apparatus for providing 5V tolerance to an output buffer operating at low voltage according to claim 17, wherein:

means for providing a power supply provides a nominal power supply of 1.8V.

20. The apparatus for providing 5V tolerance to an output buffer operating at low voltage according to claim 17, wherein:

said buffer can sink at least 48 mA of current.